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EXAMINER

LE, NHAN T

ART UNIT PAPER NUMBER

2685

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/073,029

Applicant(s)

TANAKA ET AL.

Examiner

Nhan T Le

Art Unit

2685

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 February 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-3 is/are rejected.
- 7) ☒ Claim(s) 4-10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 February 2002 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 02/12/02.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Specification

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "the," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The abstract of the disclosure is objected to because the abstract contains more than one single paragraph. Correction is required. See MPEP § 608.01(b).

Drawings

The drawings (figures 1, 4, 5, 8, 11, 12, 19) are objected to because the figures do not have element name labels associated with numbers. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief

Art Unit: 2685

description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Figure 18 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

1. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zamat et al (US 5,896,421) in view of Yochem (US 2002/0137487).

As to claim 1, Zamat teaches a direct-conversion transmitting circuit, characterized by local modulation circuit comprising first and second mixers (see fig. 3, numbers 66, 70, col. 3, lines 46-59), first and second low-pass filters (see fig. 3, number 56, col. 3, lines 10-26), and a first phase shifter (see fig. 3, number 72, col. 3, lines 46-59), wherein high frequency output terminals of the first and second mixers are connected to each other; an output terminal of the first filter is connected to an input terminal of the first mixer; a first output terminal of the first phase shifter is connected to a local signal input terminal of the first mixer; a second output terminal of the first phase shifter is connected to a local signal input terminal of the second mixer (see col. 3, lines 46-59); and input signals are applied to an input terminal (see fig. 3, I, Q), respectively. Zamat fails to teach first and second gain/bias adjustment means wherein the inputs are applied to the input terminal, the input terminal of the first low-pass filter is connected to an output terminal of the first gain/bias adjustment means; the input terminal of the second low-pass filter is connected to an output terminal of the second gain/bias adjustment means. Yochem teaches a gain/bias adjustment mean which are connected to the filter (see fig. 1, number 106, page 2, paragraphs 0019-0020) wherein the inputs are applied to the input terminal, the input terminal of the low-pass filter is connected to an output terminal of the gain/bias adjustment mean. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Yochem into the system of Zamat in order to provide power control in the linear transmission.

Art Unit: 2685

2. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zamat et al (US 5,896,421) in view of Yochem (US 2002/0137487) and further in view of Atkinson (US 6,731,923).

As to claim 2, the combination of Zamat and Yochem fails to teach a direct-conversion transmitting circuit, characterized in that the phase shifter is composed of a frequency divider circuit. Atkinson teaches a direct-conversion transmitting circuit, characterized in that the phase shifter is composed of a frequency divider circuit (see col. 3, lines 12-32). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Atkinson into the system of Zamat and Yochem in order to adjust the frequency input for phase shift device.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zamat et al (US 5,896,421) in view of Yochem (US 2002/0137487) and further in view of Younis et al (US 6,721,368).

As to claim 3, the combination of Zamat and Yochem fails to teach a direct-conversion transmitting circuit, characterized in that each circuit of the first and second low-pass filters is composed of a filter whose order is at least a second order. Younis teaches transmitting system where the low-pass filter is second order filter (see col. 10, lines 1-45). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to provide the teaching of Younis into the system of Zamat and Yochem in order to improve the response time.

Allowable Subject Matter

Claims 4-10 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim 4, the applied reference fails to teach a direct-conversion transmitting circuit, characterized in that the first and second low-pass filter circuits are each composed of a Sallen-Key type filter circuit, the Sallen-Key type filter is composed of first and second resistors, first and second capacitors, and a first transistor, and a first terminal of the first resistor is an input of the filter; a second terminal of the first resistor is connected to a first terminal of the second resistor; a second terminal of the second resistor is connected to a base of the first transistor; a first terminal of the first capacitor is connected to the second terminal of the first resistor; a second terminal of the first capacitor is connected to an emitter of the first transistor; a first terminal of the second capacitor is connected to the second terminal of the second resistor; a second terminal of the second capacitor is connected to a grounding potential; a collector of the first transistor is connected to a power source potential; and an emitter of the first transistor is an output terminal of the filter as cited in the claim.

Regarding claim 5, the applied reference fails to teach a direct-conversion transmitting circuit, characterized in that each of the first and second low-pass filter circuits is composed of two sets of first and second Sallen-Key type filter circuits, the first and second Sallen-Key type filter circuits are each composed of a first, second, third, and fourth resistors, a first and second capacitors, and a first and second transistors, a first terminal of the first resistor is an input terminal of the filter circuit; a

second terminal of the first resistor is connected to a first terminal of the second resistor; a second terminal of the second resistor is connected to a base of the first transistor; a first terminal of the first capacitor is connected to the second terminal of the first resistor; a second terminal of the first capacitor is connected to an emitter of the first transistor; a first terminal of the second capacitor is connected to the second terminal of the second resistor; a second terminal of the second capacitor is connected to a grounding potential; a collector of the first transistor is an output terminal of the filter circuit; a first terminal of the third resistor is connected to the emitter of the first transistor; a second terminal of the third resistor is connected to a grounding potential; a collector and a base of the second transistor are connected to the first terminal of the first resistor; a first terminal of the fourth resistor is connected to an emitter terminal of the second transistor; and a second terminal of the fourth resistor is connected to a grounding potential, each of the first and second gain/bias adjustment means is composed of: a first differential pair serving as a voltage/current converter circuit that converts a differential voltage into a differential current; and a second and third differential pairs comprising a first and second collector output terminals, a first and second base input terminals, and an emitter coupling input terminal, and a first collector output terminal of the first differential pair is connected to the input terminal of the first Sallen-Key filter circuit; a second collector output terminal of the first differential pair is connected to an input terminal of the second Sallen-Key filter circuit; an output terminal of the first Sallen-Key filter circuit is connected to an emitter coupling input terminal of the second differential pair; an output terminal of the second Sallen-Key filter circuit is connected to

Art Unit: 2685

an emitter coupling input terminal of the third differential pair; first collector output terminals of the second and third differential pairs are connected to each other; second collector output terminals of the second and third differential pairs are connected to each other; a second base input terminal of the third differential pair is connected to a first base input terminal of the second differential pairs; and a first base input terminal of the third differential pair is connected to a second base input terminal of the second differential pair as cited in the claim.

Regarding claim 6, the applied reference fails to teach a direct-conversion transmitting circuit, characterized in that the first and second mixers are each composed of a differential circuit, and input terminal pairs of the first and second mixers are provided with a first and second DC offset correction circuits to which output terminal pairs are connected, each of the first and second DC offset correction circuits is composed of a control means having a DA converter, an AD converter, and two outputs, one output of the control means is connected to an input terminal of the DA converter; the other output of the control means is connected to an input terminal of the AD converter; respective output pairs of the DA converter and the AD converter are connected to each other and thereby are the output terminal pairs, and the control means operates the DA converter before the direct-conversion transmitting circuit generates a signal, converts the signal to a logical signal in accordance with a magnitude of a DC component generated at each input terminal of the first and second mixers, and has a function of generating, from the AD converter, a DC level for

offsetting the DC component on the basis of a value of the logical signal and a function of storing an optimal level converted into the logical signal as cited in claims.

Regarding claim 7, the applied reference fails to teach a direct-conversion transmitting circuit, characterized in that the direct-conversion transmitting circuit is composed of: a first and second control means each having a first and second DA converters, an AD converter, and two outputs; a DC offset correction circuit having a first, second, third and fourth output terminals pairs; and further a switching means having two sets of output terminal pairs, an output of the first control means is connected to an input of the first DA converter; an output of the second control means is connected to an input of the second DA converter; an output pair of the first DA converter is connected to a first output terminal pair of the DC offset correction circuit; an output pair of the second DA converter is connected to a second output terminal pair of the DC offset correction circuit; and an output of the AD converter is connected to a third output terminal pair of the DC offset correction circuit, the first and second mixers each are composed of a differential circuit, in which the first output terminal pair of the DC offset correction circuit is connected to an input terminal pair of the first mixer; the second output terminal pair of the DC offset correction circuit is connected to an input terminal pair of the second mixer; and the third output pair of the DC offset correction circuit is connected to an input terminal pair of the switching means, one output terminal pair of the switching means is connected to the input terminal pair of the first mixer; and the other output terminal pair of the switching means is connected to the input terminal pair of the second mixer, and each of the first and second control means operates the

first and second DA converters before the direct-conversion transmitting circuit generates a signal, and converts the signal to a logical signal based on magnitude of a DC component generated at input terminals of the first and second mixers, and has a function of switching the switching means such that a DC level generated by the AD converters is applied to the input terminal pairs of the first and second mixers at a different period in order to offset a DC component generated at each of the input terminal pairs of the first and second mixers in accordance with a value of the logic signal, and a function of storing an optical level converted into the logical signal.

Regarding claim 8, the applied reference fails to teach an integrated transmitting/receiving circuit including a transmitting section and a receiving section which are integrated on the same chip, wherein the transmitting section is composed of a first direct-conversion transmitting circuit using the direct-conversion transmitting circuit according to claim 1, and a third and fourth amplifiers, and wherein the receiving section is composed of a first to third low noise amplifiers, a third and fourth mixers, a first to third frequency dividers, a first frequency synthesizer, a first voltage control type oscillator, and a first and second baseband frequency amplifiers/filter rows, the integrated transmitting/receiving circuit characterized in that an output of the first direct-conversion transmitting circuit is connected to respective input circuits of the third and fourth amplifiers; the third and fourth amplifiers are used as independent output terminals; input terminals of the first to third low noise amplifiers are connected to one another to connect inputs of the third and fourth mixers; outputs of the third and fourth mixer circuits are connected to the first and second baseband frequency amplifiers/filter

rows; a first output of the first frequency divider is connected to a local signal input terminal of the third mixer; a second output of the first frequency divider is connected to a local signal input terminal of the fourth mixer circuit; an output terminal of the first frequency synthesizer is connected to a control voltage input terminal of the first voltage control oscillator; an output of the first voltage control oscillator is connected to an input of the first frequency synthesizer; an output of the first voltage control oscillator is connected to an input terminal of the second frequency divider having two functions of executing and bypassing a frequency dividing function; the second frequency divider is connected to an input of the first frequency divider; an output of the first voltage control oscillator is connected to an input terminal of the third frequency divider having two functions of executing and bypassing a frequency dividing function; the third frequency divider is connected to an input terminal of a first phase shifter in the first direct-conversion transmitting circuit, and the first phase shifter is a frequency shifter.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Morishige et al (US 6,600,911) teaches even harmonic direct conversion receiver and transmitting and receiving apparatus using the same.

Brown et al (US 6,366,622) teaches apparatus and method for wireless communication.

Ichihara (US 2001/0051507) teaches direct conversion receiver and transceiver.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T Le whose telephone number is 703-305-4538. The examiner can normally be reached on 08:00-05:00 (Mon-Fri).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's Supervisor, Edward Urban can be reached on 703-305-4385. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Nhan Le


10-31-2004

NGUYEN T. VO
PRIMARY EXAMINER